REMARKS

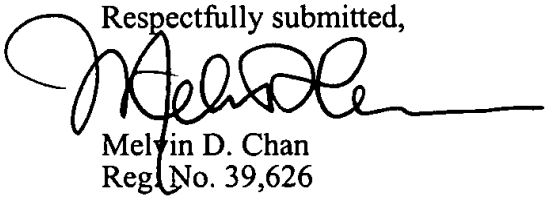
Applicants have amended the application to incorporate figures 12, 15a, 15b, 17a, and 17b of U.S. patent number 5,095,344 and their accompanying detailed description. Since the present application fully incorporates U.S. patent number 5,095,344 by reference, the inclusion of the material from U.S. patent number 5,095,344 is not new matter. The addition of the figures and accompanying description provides support for claims 68-78.

CONCLUSION

In view of the foregoing, applicants believe the application is now in a form for setting up an interference proceeding between the present application and U.S. patent number 5,818,754, as requested in applicants' Amendment and Request for Declaration of Interference mailed March 12, 2000. A prompt declaration of the requested interference is respectfully requested.

If the Examiner has any questions about this request or application, please contact the undersigned at 650-326-2400 x5213.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Page 5, lines 27-28 are amended as follows:

Fig. 8 is a block diagram illustrating the write cache circuit inside the controller[.] ;

Fig. 9 outlines the key steps in the new algorithm used to erase with a minimum stress;

Figs. 10 and 11 are schematic representations of two memory arrays for the Flash EEprom embodiments of this invention;

Fig. 12 contains Table I which shows voltage conditions for all operational modes for the array of Fig. 10; and

Fig. 13 contains Table II which shows example voltage conditions for all operational modes for the virtual ground array of Fig. 11.